ABSTRACT

A receiver unit includes a first buffer that receives and stores digitized samples at a particular sample rate and a data processor that retrieves segments of digitized samples from the first buffer and processes the retrieved segments with a particular set of parameter values. The data processor is operated based on a processing clock having a frequency that is (e.g., ten or more times) higher than the sample rate. Multiple instances of the received signal can be processed by retrieving and processing multiple segments of digitized samples from the first buffer. The receiver unit typically further includes a receiver that receives and processes a transmitted signal to provide the digitized samples and a controller that dispatches tasks for the data processor. The data processor can be designed to include a correlator, a symbol demodulation and combiner, a first accumulator, and a second buffer, or a combination thereof. The correlator despreads the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples, which are further processed by the symbol demodulation and combiner to provide processed symbols. The second buffer stores the processed symbols, and can be designed to provide de-interleaving of the processed symbols.